

Performance Engineering in HPC Application Development

Felix Wolf 27-06-2012





German Research School for Simulation Sciences

- Joint venture of
 - Forschungszentrum Jülich
 - RWTH Aachen University
- Four research laboratories
 - Computational biophysics
 - Computational engineering
 - Computational materials science
 - Parallel programming
- Education
 - M.Sc. in Simulation Sciences
 - Ph.D. program
- About 50 scientific staff members



Aachen



Jülich

Forschungszentrum Jülich



Helmholtz Center with ca. 4400 employees

Application areas

- Health
- Energy
- Environment
- Information

Key competencies

- Physics
- Supercomputing



Rheinisch-Westfälische Technische Hochschule Aachen



- 260 institutes in nine faculties
- Strong focus on engineering
- > 200 M€ third-party funding per year
- Around 31,000 students are enrolled in over 100 academic programs
- More than 5,000 are international students from 120 different countries
- Cooperates with Jülich within the Jülich Aachen Research Alliance (JARA)



University main building

Euro-Par 2013 in Aachen

- International conference series
 - Dedicated to parallel and distributed computing
- Wide spectrum of topics
 - Algorithms and theory
 - Software technology
 - Hardware-related issues





Performance



Performance optimization pays off

Example: HPC Service RWTH Aachen ~300 TFlops Bull/Intel cluster

Total cost of ownership (TCO) per year: 5.5 M€

Resource type	Fraction of TCO
Hardware	1/2
Energy	1/4
Staff	1/8
Others	1/8

Source: Bischof, an Mey, Iwainsky: Brainware for green HPC, Computer Science-Research and Development, Springer

Tuning the workload by 1% will "save" 55k€ per year ~ 1 FTE

Objectives

- Learn about basic performance measurement and analysis methods and techniques for HPC applications
- Get to know Scalasca, a scalable and portable performance analysis tool

Outline

- Principles of parallel performance
- Performance analysis techniques
- Practical performance analysis using Scalasca

Why parallelism at all? Moore's Law is still in charge...

CPU Transistor Counts 1971-2008 & Moore's Law



Source: Wikipedia

Free lunch is over...



Parallelism is crucial for optimal performance



intel

Software

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Parallelism

- System/application level
 - Server throughput can be improved by spreading workload across multiple processors or disks
 - Ability to add memory, processors, and disks is called scalability
- Individual processor
 - Pipelining
 - Depends on the fact that many instructions do not depend on the results of their immediate predecessors
- Detailed digital design
 - Set-associative caches use multiple banks of memory
 - Carry-lookahead in modern ALUs

Amdahl's Law for parallelism

 Assumption – program can be parallelized on p processors except for a sequential fraction f with

 $0 \leq f \leq 1$

$$Speedup(p) = \frac{t_s}{t_p} = \frac{1}{f + \frac{1 - f}{p}} < \frac{1}{f}$$

• Speedup limited by sequential fraction

Available parallelism

• Overall speedup of 80 on 100 processors

$$80 = \frac{1}{f + \frac{1 - f}{p}}$$

f = 0.0025

Law of Gustafson

- Amdahl's Law ignores increasing problem size
 - Parallelism often applied to calculate bigger problems instead of calculating a given problem faster
- Fraction of sequential part may be function of problem size
- Assumption
 - Sequential part has constant runtime $\tau_{\rm f}$
 - Parallel part has runtime $\tau_v(n,p)$
- Speedup

Speedup(n,p) =
$$\frac{\tau_{f} + \tau_{v}(n,l)}{\tau_{f} + \tau_{v}(n,p)}$$

If parallel part can be perfectly parallelized

Parallel efficiency

$$Efficiency(p) = \frac{Speedup(p)}{p}$$

- Metric for cost of parallelization (e.g., communication)
- Without super-linear speedup

Efficiency(p) ≤ 1

- Super-linear speedup possible
 - Critical data structures may fit into the aggregate cache

Scalability

Weak scaling

- Ability to solve a larger input problem by using more resources (here: processors)
- Example: larger domain, more particles, higher resolution
- Strong scaling
 - Ability to solve the same input problem faster as more resources are used
 - Usually more challenging
 - Limited by Amdahl's Law and communication demand

Serial vs. parallel performance

- Serial programs
 - Cache behavior and ILP
- Parallel programs
 - Amount of parallelism
 - Granularity of parallel tasks
 - Frequency and nature of inter-task communication
 - Frequency and nature of synchronization
 - Number of tasks that synchronize much higher \rightarrow contention

Goals of performance analysis

- Compare alternatives
 - Which configurations are best under which conditions?
- Determine the impact of a feature
 - Before-and-after comparison
- System tuning
 - Find parameters that produce best overall performance
- Identify relative performance
 - Which program / algorithm is faster?
- Performance debugging
 - Search for bottlenecks
- Set expectations
 - Provide information for users

Analysis techniques (1)

- Analytical modeling
 - Mathematical description of the system
 - Quick change of parameters
 - Often requires restrictive assumptions rarely met in practice
 - Low accuracy
 - Rapid solution
 - Key insights
 - Validation of simulations / measurements
- Example

- Memory delay
$$t_{avg} = ht_c + (1-h)t_m$$

- Parameters obtained from manufacturer or measurement

Analysis techniques (2)

- Simulation
 - Program written to model important features of the system being analyzed
 - Can be easily modified to study the impact of changes
 - Cost
 - Writing the program
 - Running the program
 - Impossible to model every small detail
 - Simulation refers to "ideal" system
 - Sometimes low accuracy
- Example
 - Cache simulator
 - Parameters: size, block size, associativity, relative cache and memory delays

Analysis techniques (3)

- Measurement
 - No simplifying assumptions
 - Highest credibility
 - Information only on specific system being measured
 - Harder to change system parameters in a real system
 - Difficult and time consuming
 - Need for software tools
- Should be used in conjunction with modeling
 - Can aid the development of performance models
 - Performance models set expectations against which measurements can be compared

Comparison of analysis techniques



Based on SC'11 paper from Torsten Hoefler et al.

Metrics of performance

- What can be measured?
 - A count of how many times an event occurs
 - E.g., Number of input / output requests
 - The duration of some time interval
 - E.g., duration of these requests
 - The size of some parameter
 - Number of bytes transmitted or stored
- Derived metrics
 - E.g., rates / throughput
 - Needed for normalization

Primary performance metrics

- Execution time, response time
 - Time between start and completion of a program or event
 - Only consistent and reliable measure of performance
 - Wall-clock time vs. CPU time
- Throughput
 - Total amount of work done in a given time

• Performance = 1 Execution time

- Basic principle: reproducibility
- Problem: execution time is slightly non-deterministic
 - Use mean or minimum of several runs

Alternative performance metrics

- Clock rate
- Instructions executed per second
- FLOPS

"Math" operations? HW operations? HW instructions? Single or double precision?

- Floating-point operations per second
- Benchmarks
 - Standard test program(s)
 - Standardized methodology
 - E.g., SPEC, Linpack
- QUIPS / HINT [Gustafson and Snell, 95]
 - Quality improvements per second
 - Quality of solution instead of effort to reach it

Peak performance

 Peak performance is the performance a computer is guaranteed not to exceed



Performance tuning cycle



Instrumentation techniques

• Direct instrumentation

- Measurement code is inserted at certain points in the program
 - Example: function entry/exit, dispatch or receipt of messages
- Can be done manually or automatically
- Advantage: captures all instrumented events
- Disadvantage: overhead more difficult to control
- Sampling (statistical approach)
 - Based on the assumption that a subset of a population being examined is representative for the whole population
 - Measurement performed only in certain intervals usually implemented with timer interrupt
 - Advantage: overhead can be easily controlled
 - Disadvantage: incomplete information, harder to access program state

Measurement



- Communication cost
- Synchronization cost
- IO accesses
- System calls
- Hardware events

Critical issues

- Accuracy
 - Perturbation
 - Measurement alters program behavior
 - E.g., memory access pattern
 - Intrusion overhead
 - Measurement itself needs time and thus lowers performance
 - Accuracy of timers, counters
- Granularity
 - How many measurements
 - Pitfall: short but frequently executed functions
 - How much information / work during each measurement
- Tradeoff
 - Accuracy \Leftrightarrow expressiveness of data

Single-node performance

• Huge gap between CPU and memory speed



Source: Hennessy, Patterson: Computer Architecture, 4th edition, Morgan Kaufmann

- Internal operation of a microprocessor potentially complex
 - Pipelining
 - Out-of-order instruction issuing
 - Branch prediction
 - Non-blocking caches

Hardware counters

- Small set of registers that count events
- Events are signals related to the processor's internal function
- Original purpose: design verification and performance debugging for microprocessors
- Idea: use this information to analyze the performance behavior of an application as opposed to a CPU

Typical hardware counters

Cycle count	
Instruction count	All instructions
	Floating point
	Integer
	Load / store
Branches	Taken / not taken
	Mispredictions
Pipeline stalls due to	Memory subsystem
	Resource conflicts
Cache	I/D cache misses for
	different levels
	Invalidations
TLB	Misses
	Invalidations

Profiling

- Mapping of aggregated information
 - Time
 - Counts
 - Calls
 - Hardware counters
- Onto program and system entities
 - Functions, loops, call paths
 - Processes, threads

Call-path profiling

- Behavior of a function may depend on caller (i.e., parameters)
- Flat function profile often not sufficient
- How to determine call path at runtime?
 - Runtime stack walk
 - Maintain shadow stack
 - Requires tracking of function calls


Event tracing



- Typical events
 - Entering and leaving a function
 - Sending and receiving a message

Why tracing?

- High level of detail
- Allows in-depth post-mortem analysis of program behavior
 - Time-line visualization
 - Automatic pattern search
- Identification of wait states



Obstacle: trace size



• Problem: width and length of event trace

Tracing vs. profiling

Advantages of tracing

- Event traces preserve the temporal and spatial relationships among individual events
- Allows reconstruction of dynamic behavior of application on any required abstraction level
- Most general measurement technique
 - Profile data can be constructed from event traces
- Disadvantages
 - Traces can become very large
 - Writing events to a file at runtime can cause perturbation
 - Writing tracing software is complicated
 - Event buffering, clock synchronization, ...

scalasca 🗖

- Scalable performance-analysis toolset for parallel codes
 - Focus on communication & synchronization
- Integrated performance analysis process
 - Performance overview on call-path level via call-path profiling
 - In-depth study of application behavior via event tracing
- Supported programming models
 - MPI-1, MPI-2 one-sided communication
 - OpenMP (basic features)
- Available for all major HPC platforms

Joint project of









The team



www.scalasca.org



Encyclopedia of Parallel Computing

Edited by David Padua

SPRINGER REFERENCE

- The comprehensive source of information in the field
- Published as a fully searchable and hyperlinked eReference and in hardcover

Multi-page article on Scalasca

Encyclopedia of Parallel Computing

VOLUME 1

2 Springer

David Padua

Editor-in-Chief

Installations and users

Companies

.

- Bull (France)
- Dassault Aviation (France)
- EDF (France)
- Efield Solutions (Sweden)
- GNS (Germany)
- IBM (France, Germany)
- INTES (Germany)
- MAGMA (Germany)
- RECOM (Germany)
- SciLab (France)
- Shell (Netherlands)
- SiCortex (USA)
- Sun Microsystems (USA, Singapore, India)
- Qontix (UK)
- Research / supercomputing centers
 - Argonne National Laboratory (USA)
 - Barcelona Supercomputing Center (Spain)
 - Bulgarian Supercomputing Centre (Bulgaria)
 - CERFACS (France)
 - Centre Informatique National de l'Enseignement Supérieur (France)
 - Commissariat à l'énergie atomique (France)
 - Computation-based Science and Technology Research Center (Cyprus)
 - CASPUR (Italy)
 - CINECA (Italy)
 - Deutsches Klimarechenzentrum (Germany)
 - Deutsches Zentrum f
 ür Luft- und Raumfahrt (Germany)
 - Edinburgh Parallel Computing Centre (UK)
 - Federal Office of Meteorology and Climatology (Switzerland)
 - Flanders ExaScience Lab (Belgium)
 - Forschungszentrum Jülich (Germany)
 - IT Center for Science (Finland)
 - High Performance Computing Center Stuttgart (Germany)
 - Irish Centre for High-End Computing (Ireland)
 - Institut du développement et des ressources en informatique scientifique (France)
 - Karlsruher Institut f
 ür Technologie (Germany)
 - Lawrence Livermore National Laboratory (USA)
 - Leibniz-Rechenzentrum (Germany)
 - National Authority For Remote Sensing & Space Science (Egypt)
 - National Center for Atmospheric Research (USA)

- Research/supercomputing centers (cont.)
 - National Center for Supercomputing Applications (USA)
 - National Laboratory for High Performance Computing (Chile)
 - Norddeutscher Verbund zur Förderung des Hoch- und Höchstleistungsrechnens (Germany)
 - Oak Ridge National Laboratory (USA)
 - PDC Center for High Performance Computing (Sweden)
 - Pittsburgh Supercomputing Center (USA)
 - Potsdam-Institut f
 ür Klimafolgenforschung (Germany)
 - Rechenzentrum Garching (Germany)
 - SARA Computing and Networking Services (Netherlands)
 - Shanghai Supercomputer Center (China)
 - Swiss National Supercomputing Center (Switzerland)
 - Texas Advanced Computing Center (USA)
 - Texas A&M Supercomputing Facility (USA)
 - Très Grand Centre de calcul (France)
- Universities
 - École Centrale Paris (France)
 - École Polytechnique Fédérale de Lausanne (Switzerland)
 - Institut polytechnique de Grenoble (France)
 - King Abdullah University of Science and Technology (Saudi Arabia)
 - Lund University (Sweden)
 - Lomonosov Moscow State University (Russia)
 - Michigan State University (USA)
 - Norwegian University of Science & Technology (Norway)
 - Politechnico di Milano (Italy)
 - Rensselaer Polytechnic Institute (USA)
 - Rheinisch-Westfälische Technische Hochschule Aachen (Germany)
 - Technische Universit
 ät Dresden (Germany)
 - Università degli Studi di Genova (Italy)
 - Universität Basel (Switzwerland)
 - Universitat Autònoma de Barcelona (Spain)
 - Université de Versailles St-Quentin-en-Yvelines (France)
 - University of Graz (Austria)
 - University of Oregon (USA)
 - University of Oslo (Norway)
 - University of Paderborn (Germany)
 - University of Tennessee (USA)
 - University of Tsukuba (Japan)
 - University of Warsaw (Poland)
- 9 defense-related computing centers



Wait-state analysis

- Classification
- Quantification







XNS CFD simulation application

- Computational fluid dynamics code
 - Developed by Chair for Computational Analysis of Technical Systems, RWTH Aachen University
 - Finite-element method on unstructured 3D meshes
 - Parallel implementation based on message passing
 - >40,000 lines of Fortran & C
 - DeBakey blood pump test case
 - Scalability of original version limited <1024 CPUs



Partitioned finite-element mesh

Call-path profile: Computation



Call-path profile: P2P messaging



Call-path profile: P2P sync. ops.

Trace analysis: Late sender

XNS scalability remediation

- Review of original XNS
 - Computation is well balanced
 - Real communication is very imbalanced
 - Huge amounts of P2P synchronisations
 - Grow exponentially with number of processes
- Elimination of redundant messages
 - Relevant neighbor partitions known in advance from static mesh partitioning
 - Most transfers still required at small scale while connectivity is relatively dense
 - Growing benefits at larger scales (>512)

After removal of redundant messages

XNS wait-state analysis of tuned version

(tuned version, simulation time-step loop)

MAGMAfill by MAGMASOFT® GmbH

- Simulates mold-filling in casting processes
- Scalasca used
 - To identify communication bottleneck
 - To compare alternatives using performance algebra utility
- 23% overall runtime improvement

INDEED by GNS[®] mbh

- Finite-element code for the simulation of material-forming processes
 - Focus on creation of element-stiffness matrix
- Tool workflow
 - Scalasca identified serialization in critical section as bottleneck
 - In-depth analysis using Vampir
- Speedup of 30-40% after optimization

Scalability in terms of the number of cores

- Application study of ASCI Sweep3D benchmark
- Identified MPI waiting time correlating with computational imbalance
- Measurements & analyses demonstrated on
 - Jaguar with up to 192k cores
 - Jugene with up to 288k cores

•

Brian J.N. Wylie et al.: Large-scale performance analysis of Sweep3D with the Scalasca toolset. Parallel Processing Letters, 20(4):397-414, December 2010.

Jaguar, MK = 10 (default)

Computation

Performance dynamics

- Most simulation codes work iteratively
- Growing complexity of codes makes performance behavior more dynamic – even in the absence of failures
 - Periodic extra activities
 - Adaptation to changing state of computation
- External influence (e.g., dynamic reconfiguration)

129.tera_tf

P2P communication in SPEC MPI 2007 suite

Scalasca's approach to performance dynamics

Time-series call-path profiling

- Instrumentation of the main loop to distinguish individual iterations
 - Complete call tree with multiple metrics recorded for each iteration
 - Challenge: storage requirements proportional to #iterations

Call tree

Process topology

Online compression

- Exploits similarities between iterations
 - Summarizes similar iterations in a single iteration via clustering and structural comparisons
- On-line to save memory at run-time
- Process-local to
 - Avoid communication
 - Adjust to local temporal patterns
- The number of clusters never exceeds a predefined maximum
 - Merging of the two closest ones

Zoltán Szebenyi et al.: Space-Efficient Time-Series Call-Path Profiling of Parallel Applications. In Proc. of the SC09 Conference, Portland, Oregon, ACM, November 2009.

Reconciling sampling and direct instrumentation

- Semantic compression needs direct • instrumentation to capture communication metrics and to track the call path
- Direct instrumentation may result in excessive • overhead
- New hybrid approach ٠
 - Applies low-overhead sampling to user code
 - Intercepts MPI calls via direct instrumentation
 - Relies on efficient stack unwinding
 - Integrates measurements in statistically sound manner

Zoltan Szebenyi et al.: Reconciling sampling and direct instrumentation for unintrusive call-path profiling of MPI programs. In Proc. of IPDPS, Anchorage, AK, USA. IEEE Computer Society, May 2011.

DROPS **IGPM & SC, RWTH**

Delay analysis

time

- Classification of waiting times into
 - Direct vs. indirect
 - Propagating vs. terminal
- Attributes costs of wait states to delay intervals
 - Scalable through parallel forward and backward replay of traces

David Böhme et al.: Identifying the root causes of wait states in large-scale parallel applications. In Proc. of ICPP, San Diego, CA, IEEE Computer Society, September 2010. Best Paper Award

 Performance solving 3-D magnetohydrodynamic blast wave problem on 512 processes

Zeus-MP/2 delay analysis

- Subroutine "lorentz" has highest delay costs
- Delay originates from border of central region
- Cost distribution:
 - 15.9 % short-term
 - 84.1 % long-term

Delay cost distribution across process topology

Score-P measurement system

Vampir	Scalasca			TAU			Periscope
Interactive	Perfo	Performance		data base &			Automatic
exploration	wai	wait states		data mining			classification
Tracing		Profiling		Online interface			
Score-P measurement infrastructure							
Application (MPI, OpenMP, accelerator, PGAS, hybrid)							

gns

UNIVERSITY OF OREGON

Future work

- Integrate into production version
 - Time-series compression
 - Hybrid measurement technique
 - Delay & critical-path analysis
- Further scalability improvements
- Emerging architectures and programming models
 - Accelerators
- Interoperability with 3rd-party tools
 - Common measurement library for several performance tools
- Support for performance modeling
 - Performance extrapolation
 - Multi-experiment analysis

The virtual institute in a...

• Partnership to develop advanced programming tools for complex simulation codes

VI-HPS

- Goals
 - Improve code quality
 - Speed up development
- Activities
 - Tool development and integration
 - Training
 - Support
 - Academic workshops
- <u>www.vi-hps.org</u>

Thank you!

Deutsche Forschungsgemeinschaft DFG

Bundesministerium für Bildung und Forschung

